(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 304 263**
A3

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 88307567.3

(22) Date of filing: 15.08.88

(51) Int. Cl.[5]: H01L 25/065, H01L 25/18, H01L 25/04, H01L 25/16, H01L 25/14

(30) Priority: 17.08.87 US 86140

(43) Date of publication of application: 22.02.89 Bulletin 89/08

(84) Designated Contracting States: DE FR GB NL SE

(88) Date of deferred publication of the search report: 12.09.90 Bulletin 90/37

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(54) Semiconductor chip assembly.

(57) An integrated circuit assembly includes a plurality of semiconductor chips (10,18,20,22) which are joined mechanically and electrically. The semiconductor chips are formed by the same or different device technology, and can function as different types of elements or circuits.

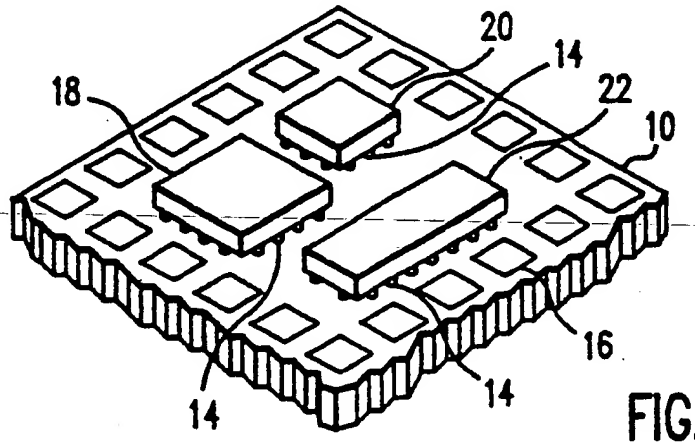

FIG. 2

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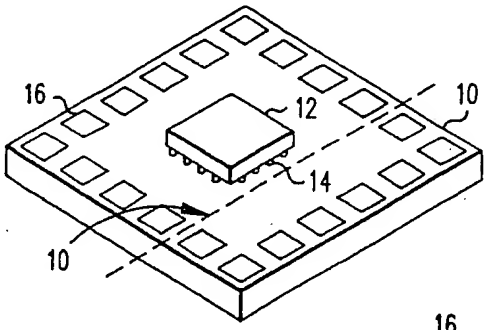

FIG. 1a

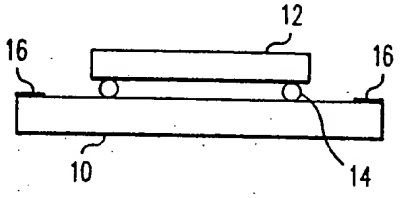

FIG. 1b

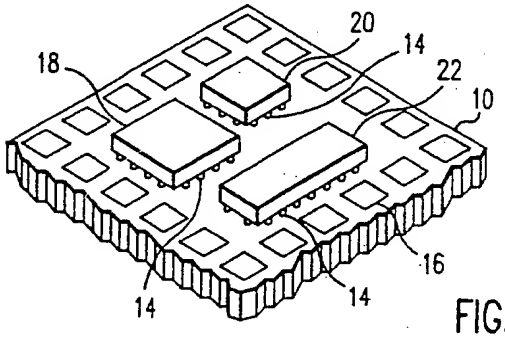

FIG. 2

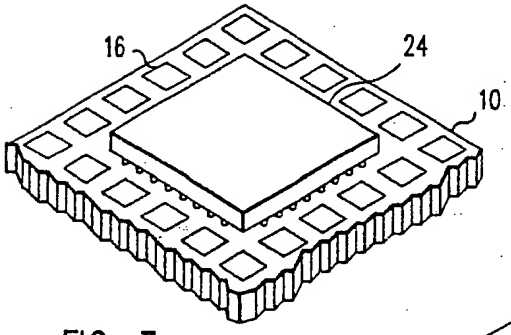

FIG. 3

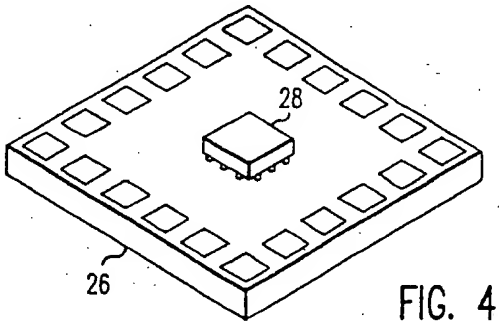

FIG. 4

attached to a mother chip.

The drawings are representations of multiplane chip assemblies to aid in the explanation of the invention and are not drawn to scale. Similar reference numerals refer to similar elements throughout the drawings.

With reference to FIGS. 1a and 1b, a semiconductor chip assembly includes an active mother chip 10, which may be formed as a CMOS (complementary metal oxide semiconductor) logic integrated circuit, and a daughter memory chip 12, which may be any type of chip desired but, for example, might be an E^2PROM (electrically erasable read only memory) or an ECL (emitter coupled logic) device. The mother chip, which serves as a carrier or support, and the daughter chip are produced separately by well known conventional processes and technology.

To implement the stacked combination of the two chips, metal or solder bumps 14 are formed on a major surface or face of either the mother chip or the daughter chip or both. The major surface is defined as the surface of the chip on which metallization or electronic circuitry is formed. The bumps are formed on circuit metallization usually referred to as bonding pads (not shown in the figures but similar to and represented by reference numeral 16) by well known methods, such as deposition and etching or by plating the material on the bond pad. The major surfaces or faces of the daughter and mother chips are aligned in registration with the solder bumps and brought into contact. The solder bumps are heated to reflow and upon cooling the daughter and mother chips become attached. The attachment of the two chips can also be effectuated by metallurgical bonding, by way of example. The solder bumps electrically and physically connect the bond pads and the circuitry of the two chips. External electrical connection to the mother chip can be made by wire bonding or by bump and lead frame attachment, etc. If bumps are used they can be formed simultaneously with the bumps used in mother to daughter connection.

In FIG. 2, a plurality of daughter chips 18, 20, 22 are joined to the mother chip 10 by metal bumps 14. In this example, the mother chip serves as a logic chip, whereas the daughter chips may encompass different technologies and function as a DRAM or SRAM (dynamic, or static random access memory), ROM (read only memory), EPROM (erasable programmable read only memory) or E^2PROM (electrically erasable PROM) or any other function desired.

An alternative embodiment is shown in FIG. 3, which includes a passive daughter chip 24 which may be used as a bus, ground plane or general interconnect. The daughter chip 24 is joined to the mother chip in the same manner described above.

With reference to FIG. 4, a carrier mother chip is provided that functions as a power transistor 26 and has an integrated circuit chip 28 attached to it by metal bumps or bonds 14.

In FIG. 5, a semiconductor chip assembly includes a mother chip 10 and a daughter chip 12 which is attached to the mother chip 10 by an attachment medium 31, which may be an epoxy adhesive, for example. The daughter chip 12 is wire bonded to bond pads 16 by means of wires 30 so that the integrated circuit of the daughter chip 12 is electrically connected to the circuitry of the mother chip 10 through the die bond pads.

FIG. 6 depicts a semiconductor device including a daughter chip 12 with one portion attached to a mother chip 10 by means of one or more solder bumps 14. In this embodiment, the daughter chip 12 projects past one end of the mother chip 10, and has an opposite portion attached to a second mother chip 10a by means of solder bumps 14a so that it straddles the chips 10 and 10a. The metallization lines forming the circuitry of the chip 12 and the chips 10 and 10a are electrically connected. Alternatively, the element 10a can be a support or substrate without an integrated circuit defined therein.

In FIG. 7, the major surface of a bridging chip 12c is attached by solder bumps 14 to spaced chips 12a and 12b. The chips 12a and 12b are disposed in the same plane and are connected respectively to the bond pads 16 of chip 10. The integrated circuitry of chip 12c is formed on its bottom surface and is electrically connected to the circuitry on the top surfaces of chips 12a and 12b and thus electrically coupled to the integrated circuit formed on the top surface of chip 10.

FIGS. 8a and 8b illustrate embodiments having vertical stacks of semiconductor chips, each of which can be formed of a different technology, for example, bipolar, CMOS, RAM or logic devices, and each of which can have different applications or functions. In FIG. 8a, e.g., a first daughter chip 12a is joined to one surface of a mother chip 10 by an attachment medium, and a second daughter chip 12b is joined to the major surface of chip 12a by solder bumps 14. The circuitry of the chip 10 is electrically connected to the circuitry of the chip 12a by bond wires 30, whereas the circuitry of chip 12a is connected to the metallization lines on the major surface of chip 12b by the conductive solder.

Similarly, the assembly of FIG. 8b embodies a stack of chips 10, 12a and 12b, preferably of different technologies, wherein the chips are joined by solder bumps 14a and 14b. The major surface of chip 12a having the integrated circuit formed thereon can be selectively attached to either of the major surfaces of chip 10 or chip 12b on which metallization lines are formed, in which case chip 12a has conductive elements on both the front and back faces with electric connection between front and back. FIG. 9 illustrates a non-parallel attachment of one or more chips to a mother chip. In this case, the bumps 14 are formed on the edge of the chips and attached to the mother chip 10.

By virtue of the novel assembly disclosed herein, it is possible to mix discrete devices with integrated circuits. Conventional technology utilizing metal bumps or metallurgical bonding is used to join and interconnect the semiconductor chips. Memory chips that are manufactured in large volume and at low cost are easily integrated into a custom logic circuit using the approach described herein. Very high speed bipolar memories can be integrated into a logic chip so that signals being processed do not go "off chip" into the memory, which is "on chip".

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(54) Semiconductor chip assembly.

(57) An integrated circuit assembly includes a plurality of semiconductor chips (10,12;10,18,20,22;10,24;26,28; 10,100,12;10,12a,12b,12c) which are joined mechanically and electrically. The semiconductor chips are formed by the same or different device technology, and can function as different types of elements or circuits.

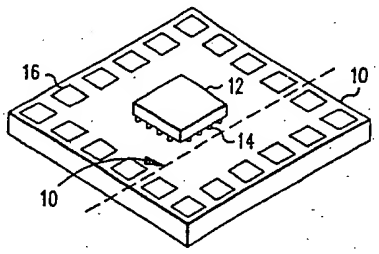


FIG. 1a

EP 0 304 263 A2

Patent Abstracts of Japan

PUBLICATION NUMBER : 07321152
PUBLICATION DATE : 08-12-95

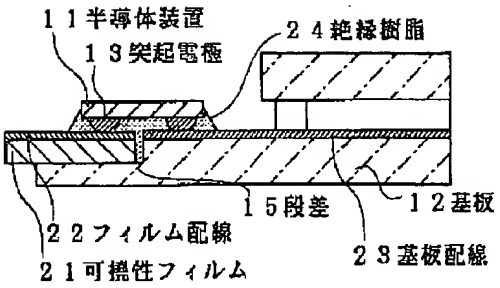
APPLICATION DATE : 28-03-95
APPLICATION NUMBER : 07069268

APPLICANT : CITIZEN WATCH CO LTD;

INVENTOR : KIKUCHI MASAYOSHI;

INT.CL. : H01L 21/60 G02F 1/1345 H05K 1/18

TITLE : SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF



ABSTRACT : PURPOSE: To enable the bump electrode of a semiconductor device to be directly connected to the film wiring of a flexible film by a method wherein a step is provided to a board possessed of a board wiring, a flexible film possessed of a film wiring is bonded to the step, and a semiconductor device is provided spreading over the flexible film and the board.

CONSTITUTION: A film wiring 22 is provided onto the upside of a flexible film 21. A flexible film 21 is so mounted on the tread of a step 15 provided to a board 12 as to make the upside of film wiring 22 flush with that of a board wiring 23. Bump electrodes 13 serving as input/output terminals are provided to the semiconductor device 11. The semiconductor device 11 is provided stretching over the board 11 and the film wiring 22. A connection between the semiconductor device 11 and both the film wiring 22 and the board wiring 23 is made by bringing the bump electrodes 13 into contact with both the film wiring 22 and the board wiring 23 respectively. An intsulating resin 24 is interposed between the semiconductor device 11 and both the board 12 and the flexible film 21.

Patent Abstracts of Japan

PUBLICATION NUMBER : 06230405
PUBLICATION DATE : 19-08-94

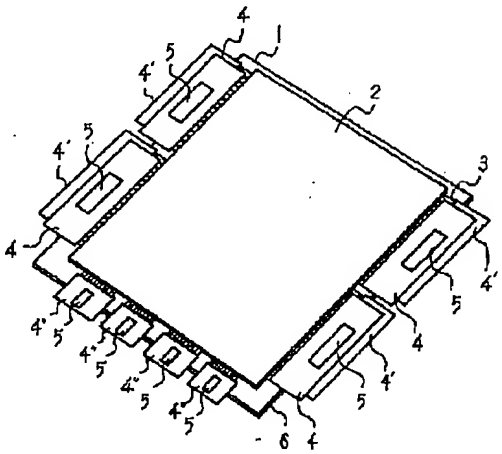
APPLICATION DATE : 04-02-93
APPLICATION NUMBER : 05017147

APPLICANT : NEC CORP;

INVENTOR : OKUBO HIROSHI;

INT.CL. : G02F 1/1345 G09G 3/18

TITLE : LIQUID CRYSTAL DISPLAY DEVICE



ABSTRACT : PURPOSE: To provide a connecting structure capable of connecting TCP which is a driver IC and, heretofore, difficult to be connected by reduction in wiring pitches following heightening the fineness of the liquid crystal display device.

CONSTITUTION: The output leads of the tape carrier package(TCP) which is a driver IC formed to the wiring pitch of integer times the wiring pitch of external leading-out electrodes 3 wired from the image display part 2 of the liquid crystal display device, are formed and area aligned and connected to these external leading-out electrodes in the form of bestriding the electrodes. The output wirings of another TCP are similarly aligned and connected to the positions of the external leading-out electrodes shifted by one pitch. Consequently, the reduction of the wiring pitch of the external leading-out electrodes down to 0.03mm is possible. The driver IC of the completed liquid crystal display device is in the form of superposing the TCPs double.

Patent Abstracts of Japan

PUBLICATION NUMBER : 05173160
PUBLICATION DATE : 13-07-93

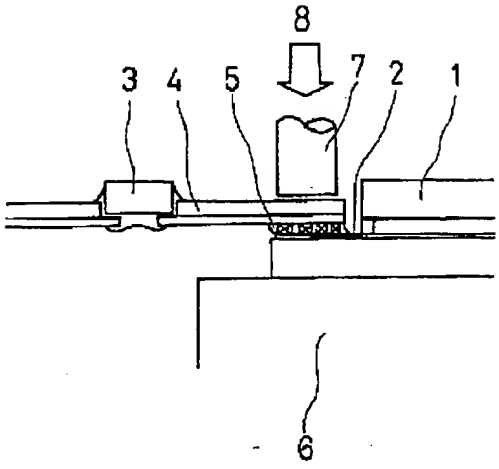
APPLICATION DATE : 24-12-91
APPLICATION NUMBER : 03341342

APPLICANT : SEIKO EPSON CORP;

INVENTOR : TAKEI SHOTARO;

INT.CL. : G02F 1/1345

TITLE : LIQUID CRYSTAL DISPLAY DEVICE AND ITS MANUFACTURE



ABSTRACT : PURPOSE: To prevent connection terminals for connection by crimping from shifting in position and to prevent a short circuit and a current leak and obtain high-level picture quality by selecting pressure and temperature at the time of heat crimping in two stages.

CONSTITUTION: A driving IC 3 is mounted on a substrate 4 that is desired and manufactured relatively to a terminal electrode 2 which is made of ITO and lead out of a picture element electrode arranged on the surface of the glass substrate constituting the liquid crystal display panel 1; and terminal electrodes are connected by heat crimping across an anisotropic conductive adhesive film 5 while sufficiently aligned. In this case, they are held at low pressure in the 1st stage and then held at specific high pressure in the 2nd stage to perform the heat crimping. Consequently, the signal from the driving IC 3 is sent from the electric conductor of the substrate 4 in the order of the terminal electrode, anisotropic conductive adhesive film 5, terminal electrode 2, and a picture element to make a display on the liquid crystal display panel 1.

XP-002076742

H01L 23/14
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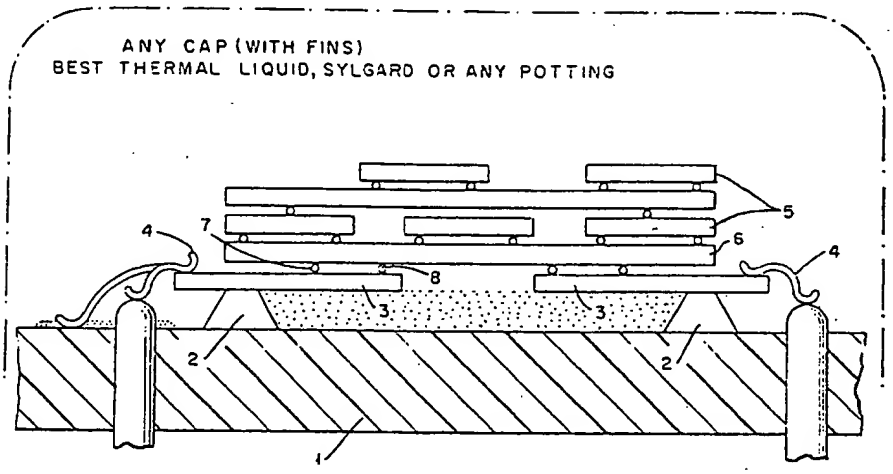
p. 2018 = 1

INTEGRATED CIRCUIT CHIP PACKAGE

C. N. Liu, D. A. Panner and K. P. Stuby



An integrated circuit chip or wafer package structure is described which permits packaging a plurality of semiconductor chips or wafers on the same substrate, while reducing the adverse affects of different coefficients of thermal expansion between the chip and the substrate.

The figure shows a substrate 1 having a first coefficient of thermal expansion upon which is attached the rigid pedestal 2. Mounted on top of the rigid pedestal 2 is the semiconductor wafer 3. Wafer 6 is mounted on top of wafers 3 by the solder ball joints 7 and 8, which transfer a mechanical moment from wafer 6 to wafer 3 in a cantilever fashion. Electrical contact between the substrate 1 and the wafer 3 is made by wire bond 4. The cantilever suspension for the wafer 3 reduces many of the thermally induced stresses imposed by prior art packaging arrangements.

The cantilever structure can serve as the base for a stacked configuration of semiconductor chips 5 as is shown. Two or more cantilever structures can serve as the base upon which a plurality of integrated circuit chips can be stacked. In an alternative configuration, the semiconductor wafer 3 can be annular in shape and make use of a plurality of rigid pedestals 2 to support the stacked configuration of chips 5 shown in the figure, which will be resistive to thermally induced stresses.